WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device comprising the steps of forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween; implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form dopant diffused regions in the semiconductor substrate on both sides of the gate electrode; and forming a silicon oxide film covering the gate electrode; and anisotropically etching the silicon oxide film to form a sidewall spacer including the silicon oxide film on the side wall of the gate electrode,

in the step of forming the silicon oxide film, the silicon oxide film being formed by thermal CVD at a 500 - 580 °C film forming temperature, using bis(tertiary-butylamino)silane and oxygen as raw materials.

2. A method for fabricating a semiconductor device comprising the steps of forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween; implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form a dopant diffused region in the semiconductor substrate on both sides of the gate electrode; and forming a silicon oxide film covering the gate electrode; and anisotropically etching the silicon oxide film to form a sidewall spacer including the silicon oxide film on the side wall of the gate electrode,

in the step of forming the silicon oxide film, the silicon oxide film being formed by thermal CVD at a 560 - 580 °C film forming temperature, using tetra-ethyl-ortho-silicate and oxygen as raw materials.

3. A method for fabricating a semiconductor device comprising the steps of forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween; implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form a dopant diffused region in the semiconductor substrate on both sides of the gate electrode; and forming a silicon oxide film covering the gate electrode; and anisotropically etching the silicon oxide film to form a sidewall spacer including the silicon oxide film on the side wall of the gate electrode,

in the step of forming the silicon oxide film, the silicon oxide film being formed by thermal CVD at a 600 - 700 °C film forming temperature for a period of film forming time of below 15 minutes, using silane and nitrous oxide as raw materials.

4. A method for fabricating a semiconductor device comprising the steps of forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween; implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form a dopant diffused region in the semiconductor substrate on both sides of the gate electrode; and forming a silicon oxide film covering the gate electrode; and anisotropically etching the silicon oxide

film to form a sidewall spacer including the silicon oxide film on the side wall of the gate electrode,

in the step of forming the silicon oxide film, the silicon oxide film beig formed by thermal CVD at a 480 - 500 °C film forming temperature for a period of film forming time of below 30 minutes, using TEOS and ozone as raw materials.

5. A method for fabricating a semiconductor device comprising the steps of forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween; implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form a dopant diffused region in the semiconductor substrate on both sides of the gate electrode; and forming a silicon oxide film covering the gate electrode; and anisotropically etching the silicon oxide film to form a sidewall spacer including the silicon oxide film on the side wall of the gate electrode,

in the step of forming the silicon oxide film, the silicon oxide film being formed by thermal CVD at a 500 - 530 °C film forming temperature for a period of film forming time of below 30 minutes, using disilane and nitrous oxide.

6. A method for fabricating a semiconductor device according to claim 1,

which further comprises, after the step of forming the silicon oxide film and before the step of forming the sidewall spacer, the step of forming a silicon nitride film covering the silicon oxide film; and in which

in the step of forming the silicon nitride film, the silicon nitride film is formed by thermal CVD at a 550 - 580 °C film forming temperature, using bis(tertiary-butylamino)silane and ammonium as raw materials,

in the step of forming the sidewall spacer, the silicon nitride film and the silicon oxide film being anisotropically etched to form the sidewall spacer including the silicon oxide film and the silicon nitride film on the side wall of the gate electrode.

7. A method for fabricating a semiconductor device according to claim 1,

which further comprises, after the step of forming the silicon oxide film and before the step of forming the sidewall spacer, the step of forming a silicon nitride film covering the silicon oxide film; and in which

in the step of forming the silicon nitride film, the silicon nitride film is formed by thermal CVD at a 650 - 700 °C film forming temperature for a period of film forming time of below 15 minutes, using silane and ammonium as raw materials,

in the step of forming the sidewall spacer, the silicon nitride film and the silicon oxide film being anisotropically etched to form the sidewall spacer including the silicon oxide film and the silicon nitride film on the side wall of the gate electrode.

8. A method for fabricating a semiconductor device comprising the step of forming an insulation film of SiN, SiCN

or SiOCN, using a first raw material of a compound containing at least silicon and nitrogen, and a second raw material of a compound containing a plurality of nitrogen atoms in a molecule.

9. A method for fabricating a semiconductor device according to claim 8, which further comprises, after the step of forming the insulation film, the steps of:

forming a gate electrode on a semiconductor substrate with a gate insulation film formed therebetween, and

implanting a dopant into the semiconductor substrate with the gate electrode as a mask to form a dopant diffused regions in the semiconductor substrate on both sides of the gate electrode; and in which

in the step of forming the insulation film, the insulation film is formed on the semiconductor substrate, covering the gate electrode; and which further comprises, after the step of forming the insulation film, the step of:

anisotropically etching the insulation film to form a sidewall spacer including the insulation film on the side wall of the gate electrode.

10. A method for fabricating a semiconductor device according to claim 9,

which further comprises, after the step of forming dopant diffused regions in the semiconductor substrate on both sides of the gate electrode and before the step of forming the insulation film, the step of forming a silicon oxide film on the semiconductor substrate, covering the gate electrode, and

in which in the step of forming the sidewall spacer, the insulation film and the silicon oxide film are anistoropically etched to form the sidewall spacer including the silicon oxide film and the insulation film on the sidewall of the gate electrode.

11. A method for fabricating a semiconductor device according to claim 8, which further comprises, before the step of forming the insulation film, the steps of:

forming a transistor on a semiconductor substrate; and

forming another insulation film on the semiconductor substrate, covering the transistor, and in which

in the step of forming the insulation film, the insulation film is formed covering said another insulation film.

12. A method for fabricating a semiconductor device according to claim 11, which further comprises, after the step of forming the insulation film, the steps of:

forming further another insulation film whose etching characteristics are different from those of said insulation film;

forming a trench down to said insulation film in said further another insulation film; and

burying an interconnection in the trench.

13. A method for fabricating a semiconductor device according to claim 8, which comprises, before the step of forming the insulation film, the steps of:

forming a transistor on a semiconductor substrate;

forming another insulation film on the semiconductor substrate, covering the transistor; and

forming further another insulation film above said another insulation film; and in which

in the step of forming the insulation film, said insulation film is formed covering said further another insulation film; and

the method further comprises, after the step of forming the insulation film, the steps of:

forming a trench in said insulation film and said further another insulation film;

forming a conducting film in the trench and on said insulation film; and

polishing the conducting film until said insulation film is exposed to form an interconnection of the conducting film in the trench.

14. A method for fabricating a semiconductor device according to claim 8, which further comprises, before the step of forming the insulation film, the steps of:

forming a transistor on a semiconductor substrate;

forming another insulation film on the semiconductor substrate, covering the transistor;

forming further another insulation film above said another insulation film; and

burying an interconnection in said further another insulation film, and in which

in the step of forming the insulation film, the insulation film is formed on said further another insulation film and the

interconnection.

15. A method for fabricating a semiconductor device according to claim 9, wherein

in the step of forming the insulation film, the insulation film is formed by thermal CVD or plasma enhanced CVD.

16. A method for fabricating a semiconductor device according to claim 8, wherein

in the step of forming the insulation film, the insulation film is formed using an additional third raw material of NH_3.

17. A method for fabricating a semiconductor device according to claim 8, wherein

the first raw material is bis(tertiary-butylamino)silane.

18. A method for fabricating a semiconductor device according to claim 8, wherein

the second raw material is a hydrazine compound or an azido compound.

19. A method for fabricating a semiconductor device according to claim 8, wherein

in the step of forming the insulation film, the insulation film is formed at a film forming temperature of below 550 °C.

20. A method for fabricating a semiconductor device according to claim 1,

which further comprises, after the step of forming the siedewall spacer, the step of implanting a dopant into the semiconductor substrate with the gate electrode and the sidewall

spacer as a mask to form dopant diffused regions a carrier concentration of which is higher and which are deeper than said dopant diffused regions.

21. A method for fabricating a semiconductor device according to claim 9,

which further comprises, after the step of forming the siedewall spacer, the step of implanting a dopant into the semiconductor substrate with the gate electrode and the sidewall spacer as a mask to form dopant diffused regions a carrier concentration of which is higher and which are deeper than said dopant diffused regions.

22. A method for fabricating a semiconductor device according to claim 1, which further comprises, after the step of forming the gate electrode and before the step of forming the dopant diffused regions, the steps of:

forming another sidewall spacer on the side wall of the gate electrode;

implanting a dopant in the semiconductor substrate with the gate electrode and said another sidewall spacer as a mask to form dopant diffused regions a carrier concentration of which is higher and which is deeper than said dopant diffused regions; and

etching off said another sidewall spacer.

23. A method for fabricating a semiconductor device according to claim 9, which further comprises, after the step of forming the gate electrode and before the step of forming

the dopant diffused regions, the steps of:

forming another sidewall spacer on the side wall of the gate electrode;

implanting a dopant in the semiconductor substrate with the gate electrode and said another sidewall spacer as a mask to form dopant diffused regions a carrier concentration of which is higher and which is deeper than said dopant diffused regions; and

etching off said another sidewall spacer.

24. A method for fabricating a semiconductor device according to claim 1,

which further comprises the step of forming pocket regions of a conduction type opposite to that of said dopant diffused regions adjacent to said dopant diffused region after the step of forming a gate electrode and before the step of forming dopant diffused regions, or after the step of forming dopant diffused regions and before the step of forming the silicon oxide film.

25. A method for fabricating a semiconductor device according to claim 9,

which further comprises the step of forming pocket regions of a conduction type opposite to that of said dopant diffused regions adjacent to said dopant diffused region after the step of forming a gate electrode and before the step of forming dopant diffused regions, or after the step of forming dopant diffused regions and before the step of forming the insulation film.